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DESIGN AND ANALYSIS OF PD-PWM MULTILEVEL INVERTER WITH REDUCED SWITCH COUNT

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Abstract- This study proposes a single-phase, 9-level, multilevel inverter (MLI) topology. The multicarrier, Phase Disposition (PD) Pulse Width Modulation (PWM) scheme is employed to generate the gating signals for the power switches. By controlling the modulation index, the desired number of levels: 3, 5, 7 and 9 of the inverter's output voltage can be achieved. For modulation index of: 0.2, 0.4, 0.6 and 0.8, the proposed inverter configuration was subjected to an R–L load and the respective numbers of output voltage level were synthesized. The topology is self-voltage balanced across the series connected capacitors. The proposed approach helps in reducing the number of independent dc voltage sources. Also the harmonic content in the output voltage is very less when compared with conventional topologies. For a modulation index of 0.8, a Total Harmonic Distortion value of 14.03% has been achieved. To verify the performance of the proposed inverter architecture, simulations and experiments are carried out on inverter for an R–L load; and adequate results are presented.
Keywords – Multilevel Inverter (MLI); Phase Disposition (PD); Pulse Width Modulation (PWM); Total Harmonic Distortion (THD)

1. INTRODUCTION

Multilevel power conversion has become increasingly popular in recent years due to advantages of high power quality waveforms, low electromagnetic compatibility concerns, low switching losses, and high-voltage capability. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost. There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design. This was followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Several combinational designs have also emerged some involving cascading the fundamental topologies.

Half and Full bridge inverters requires large input and output filters, lower voltage operating capability, harmonic distortion is high, high Electro Magnetic Interference (EMI) [2]. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. The multilevel inverters are mainly classified as diode clamped, Flying capacitor inverter and cascaded multilevel inverter. The main drawbacks of NPC inverter topology, with a level number higher than 3, is the necessity of a capacitor voltage balancing control circuit and the high voltage across the clamped diodes. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor, but needs separate dc voltage sources for each H bridges [3]. Among conventional multilevel inverters, cascaded H-bridge multilevel inverter (CHB) is one of the best approaches to increase the number of output voltage levels. As CHB increases H-bridge cells, it also increases the number of switches and also independent dc input voltage sources. One of the solutions to reduce the number of component in CHB is to use asymmetrical dc voltage sources. But the main disadvantage of asymmetric cascaded H-bridge inverter is the requirement of asymmetric DC sources for its operation. Using H Bridge with Multiple Transformer reduces the number of switches and provides proper isolation. It also uses a combination of asymmetrical voltage sources to synthesize multilevel output voltages. This technique employs only a single dc voltage source. But it uses two low frequency transformers and thus makes the system bulky and costly [6]. In case of CHB with single voltage source, capacitor acts as a DC power source. This method requires a complete monitoring of capacitor charging and discharging [7]. Modular multilevel converter was introduced in [8]. Although it is very easy to be extended to higher levels, it increases the number of bulky capacitors and switches as level increases. Most of the commonly used methods employ series connected capacitors, as it reduces the use of independent dc sources.

One of the modulation strategies for these multilevel inverter topologies is the sinusoidal pulse width modulation (SPWM), extended to multiple carrier arrangements of two types: level shifted, also known as phase disposition (PD-PWM), and phase shifted (PS-PWM); other established modulation methods include the multilevel space vector and multilevel selective harmonic elimination. Multi-reference single carrier SPWM helps in reducing the THD content in output voltage, so it is used here over multi-carrier single reference SPWM [10].

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In this work, a single sourced nine level inverter with less number of components is introduced. A multi carrier single reference PD-PWM technique is used so that it reduces the THD in output voltage. Operational principles and switching functions are analyzed. Simulation and experimental results are presented to verify the validity of the proposed inverter.

2.CONFIGURATION AND OPERATIONAL PRINCIPLE OF THE PROPOSED INVERTER

2.1. Circuit Configuration –

The circuit configuration of the proposed 9-level inverter is shown in Fig. 1.

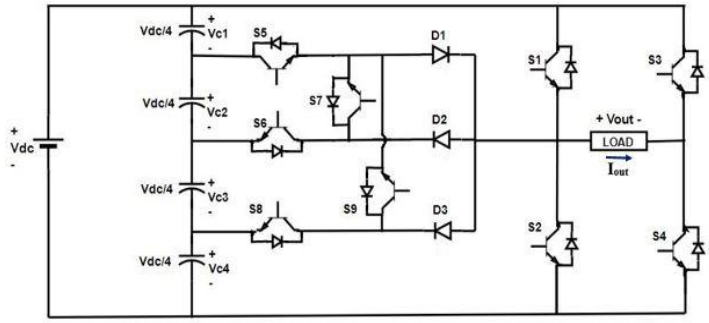


Figure 1. Circuit configuration of the 9-level PWM inverter

It has a single dc voltage source, which is that all components are ideal and the circuit is in a steady-state. Each capacitor voltage equals to Vdc/4. Then we can obtain 9 levels in the output voltage wave; Vdc, 3Vdc/4, 2Vdc/4, Vdc/4, 0, -Vdc/4, -2Vdc/4, -3Vdc/4, -Vdc. Switches in an H-bridge cell (S1 - S4) work to determine the polarity of the output voltage with the highest (or lowest) voltage level, Vdc (or -Vdc). Other voltage levels are generated by working of S5, S6, S7, S8 and S9.By varying the modulation index different voltage levels can be achieved. For this, the proposed multilevel inverter needs a single dc voltage source with a series connection of four capacitors, three diodes, nine active switches for synthesizing output voltage levels, and an H bridge cell. Also the harmonic content in the output voltage is very less when compared with conventional topologies.

The principle of PDPWM technique is to use the several carriers with single modulating waveform. In phase disposition all the carriers are in same phase above and below zero reference lie. All the carriers are in same phase in this method of PWM. It provides load voltage and current with lower harmonic distortion.

2.2. Switching scheme for 9-level inverter –

Multicarrier phase disposition PWM scheme is employed in the generation of the gating signals. Basic principle of the proposed switching strategy is to generate gate signals by comparing the rectified sinusoidal modulating/reference signal, at the fundamental frequency, with four triangular carrier waves having higher switching frequency and in-phase, but different offset voltages. Figure 2, a general PD switching scheme for controlling of the proposed 9-level PWM inverter.

For one cycle of the fundamental frequency, the proposed multilevel inverter operates through eight modes. Figure2 illustrates the per unit output voltage waveform for one cycle.

The eight modes are described as follows

Mode 1: $P_1 = 0 < \omega t < \theta_1$ and $P_7 = \theta_6 < \omega t < \pi$

Mode 2: $P_2 = \theta_1 < \omega t < \theta_2$ and $P_6 = \theta_5 < \omega t < \theta_6$

Mode 3: $P_3 = \theta_2 < \omega t < \theta_3$ and $P_5 = \theta_4 < \omega t < \theta_5$

Mode 4: $P_4 = \theta_3 < \omega t < \theta_4$

Mode 5: $P_8 = \pi < \omega t < \theta_7$ and $P_{14} = \theta_{12} < \omega t < 2\pi$

Mode 6: $P_9 = \theta_7 < \omega t < \theta_8$ and $P_{13} = \theta_{11} < \omega t < \theta_{12}$

Mode 7: $P_{10} = \theta_8 < \omega t < \theta_9$ and $P_{12} = \theta_{10} < \omega t < \theta_{11}$

Mode 8: $P_{11} = \theta_9 < \omega t < \theta_{10}$

Table I. Output voltage according to the switches on-off conditions

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_{OUT}
On	Off	Off	On	Off	Off	Off	Off	Off	+Vdc
Off	Off	Off	On	On	Off	Off	Off	Off	+3Vdc/4
Off	Off	Off	On	Off	Off	On	Off	Off	+2Vdc/4
Off	Off	Off	On	Off	Off	Off	Off	On	+Vdc/4
Off	On	Off	On	Off	Off	Off	Off	Off	0
Off	Off	On	Off	Off	Off	On	Off	Off	-Vdc/4
Off	Off	On	Off	Off	On	Off	Off	Off	-2Vdc/4
Off	Off	On	Off	Off	Off	Off	On	Off	-3Vdc/4
Off	On	On	Off	Off	Off	Off	Off	Off	-Vdc

By comparison of the reference and each carrier wave, it produces command signals C_a, C_b, C_c and C_d. When V_{T1}, V_{T2} and V_{T3} are lower than V_{ref}, then C_a, C_b, andC_c become one, and when V_{T4} higher than V_{ref}, then C_d becomes one. By logical combination of C_a, C_b, C_c, C_d and P_n it generates switching signals (S_n).

The phase angle θ, depends on the modulation index (M_a)

$$M_a = \frac{A_m}{4A_c} \quad (1)$$

Where, A_c - is the peak-to-peak value of the triangular carrier signals, A_m- is the peak value of the rectified sinusoidal reference signal.

For M_a equal to or less than 0.25 ($M_a \leq 0.25$), only the lower triangular carrier signal V_{T1}, is compared with the reference wave. The output voltage consists of three voltage levels. If M_a is greater than 0.25 and less than 0.5 ($0.25 < M_a \leq 0.5$), two carrier signals $V_{T1}$and V_{T2}, are compared with the reference wave. The output voltage consists of five voltage levels. When M_a is more than 0.5 but less than 0.75 ($0.5 < M_a \leq 0.75$), three carrier signals V_{T1}, V_{T2} and V_{T3}, are compared with the reference. The output voltage consists of seven voltage levels. If M_a is set to be greater than 0.75 ($M_a > 0.75$), four carrier signals V_{T1}, V_{T2}, V_{T3} and V_{T4} are compared with the reference. The output voltage consists of nine voltage levels. In this case, all the four carrier signals, V_{T1}-V_{T4} have to be compared with the reference to produce switching signals for the power switches.

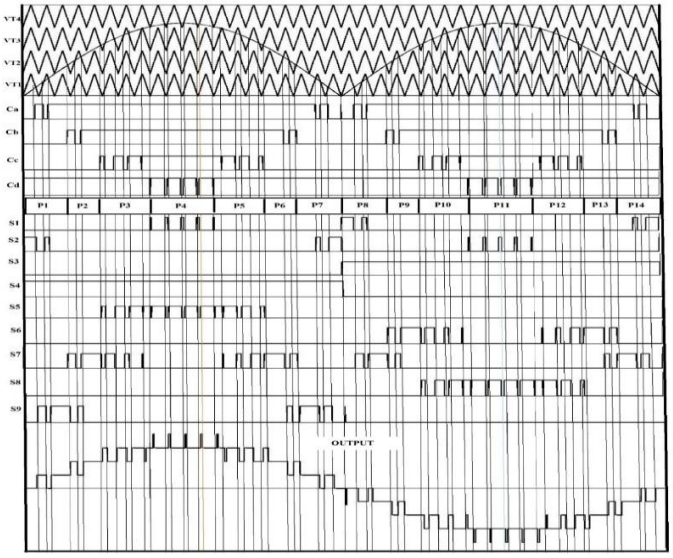


Figure. 2. Switching pattern for generating 9-level output voltage

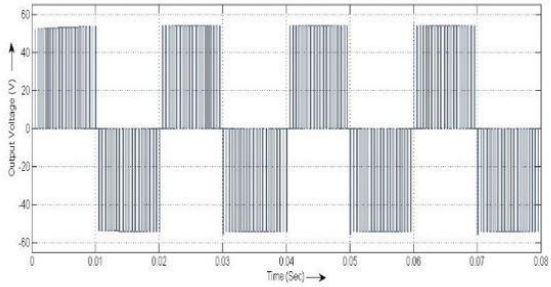
The period (P_n) of each mode varies in terms of switching angle n, which is determined by modulation index (M_a). By using logical expressions AND, OR and NOT each switching signal is determined and simulated.

$$S_1 = C_a.(P_8 + P_{14}) + C_d.P_4 \quad (2)$$
$$S_2 = C_a.(P_1 + P_7) + C_d.P_{11} \quad (3)$$
$$S_3 = P_8 + P_9 + P_{10} + P_{11} + P_{12} + P_{13} + P_{14} \quad (4)$$
$$S_4 = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 \quad (5)$$
$$S_5 = C_c.(P_3 + P_5) + C_d.P_4 \quad (6)$$
$$S_6 = C_b.(P_9 + P_{13}) + C_c.(P_{10} + P_{12}) \quad (7)$$
$$S_7 = C_a.(P_8 + P_{14}) + C_c.(P_3 + P_5) + C_b.(P_9 + P_{13}) + C_b.(P_1 + P_2 + P_6 + P_7) \quad (8)$$
$$S_8 = C_c.(P_{10} + P_{12}) + C_d.P_{11} \quad (9)$$
$$S_9 = C_a.(P_1 + P_7) + C_b.(P_2 + P_6) \quad (10)$$

3. EXPERIMENT AND RESULT

3.1. Simulation Studies and Results –

In order to access the validity of the proposed cascaded multilevel inverter topology, simulations are normally carried out in advance. MATLAB SIMULINK simulated the proposed 9-level inverter in accordance to the switching scheme presented in Table I. The PWM switching patterns are generated by comparing four disposed triangular carriers, V_{T1}-V_{T4}at switching frequency of 2 kHz against a rectified sinusoidal reference wave at fundamentalfrequency of 50 Hz, as depicted in Figure 2. Actually, the proposed topology inverter configuration is capable of synthesizing 3-, 5-, 7- and 9-level output voltagewaveforms for an RL load, depending on the value of themodulation index at Vs = 220V, R = 50Ω, L = 10mH. The voltage across series connected capacitors is found in the Fig. 11. It is found that the voltages are balanced at the voltage Vdc/4. This circuit is found to be self-balanced and no modified switching scheme is needed to balance the capacitor voltage.



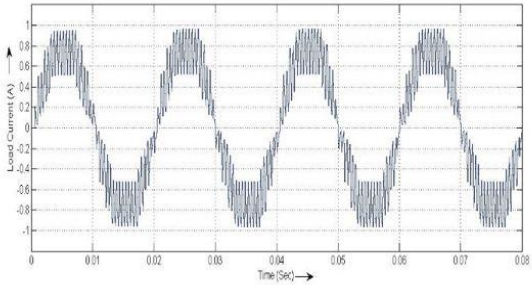
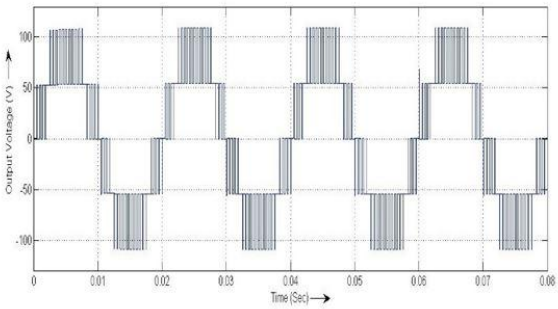


Figure 3. Simulation results of output voltage for M_a= 0.2Figure 4. Simulation results of output current for M_a= 0.2



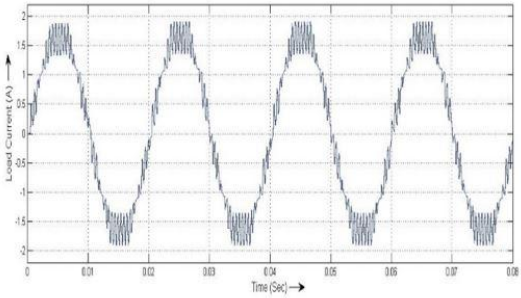
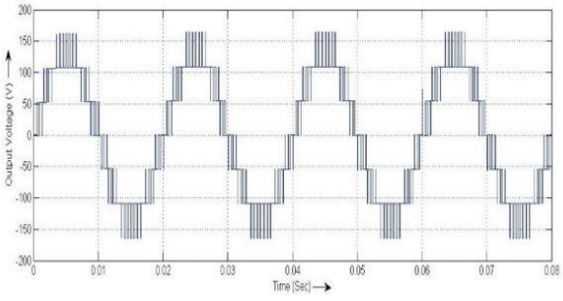


Figure 5. Simulation results of output voltage for M_a= 0.4Figure 6. Simulation results of output current for M_a= 0.4



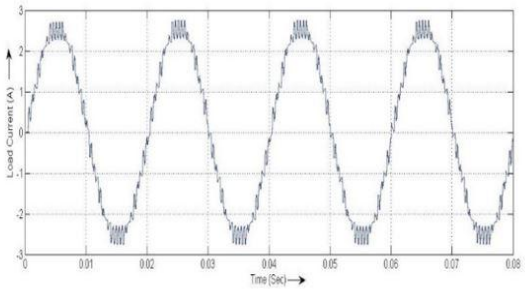


Figure 7. Simulation results of output voltage for M_a= 0.6 Figure 8. Simulation results of output current for M_a= 0.6

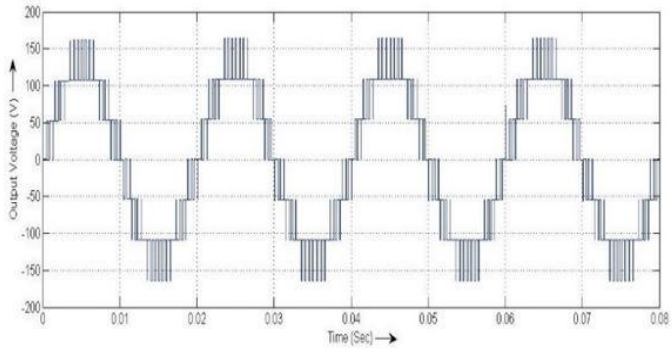


Figure9. Simulation results of output voltage for M_a= 0.8

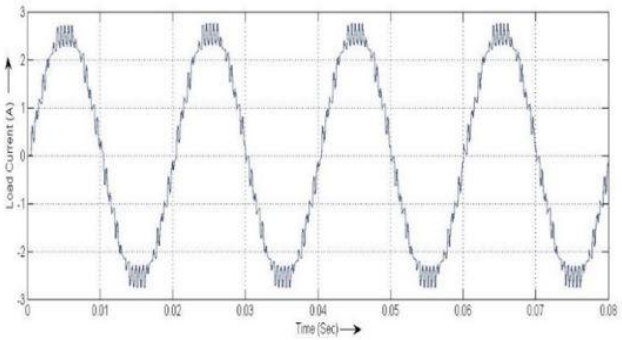


Figure 10. Simulation results of output current for M_a= 0.8

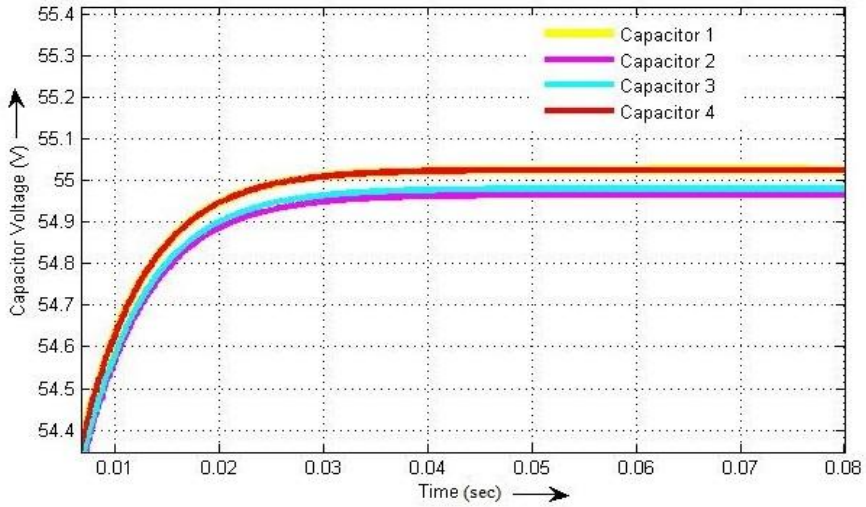
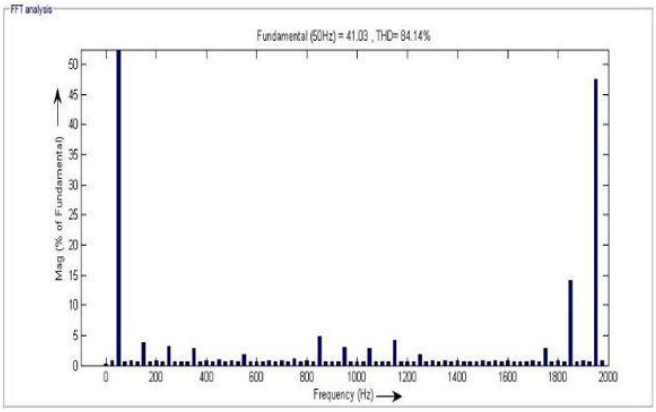


Figure 11. Simulation results for capacitor voltage balancing with PD switching scheme



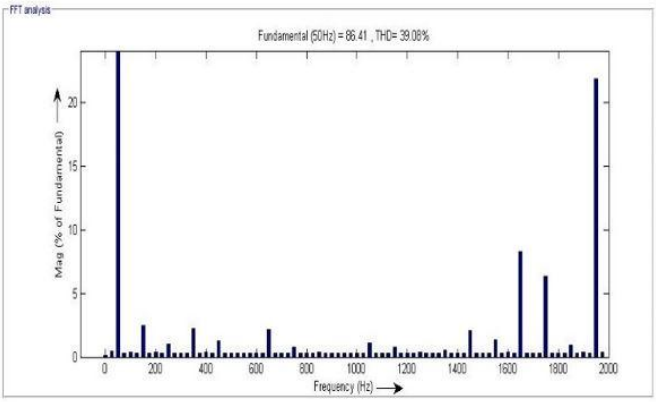
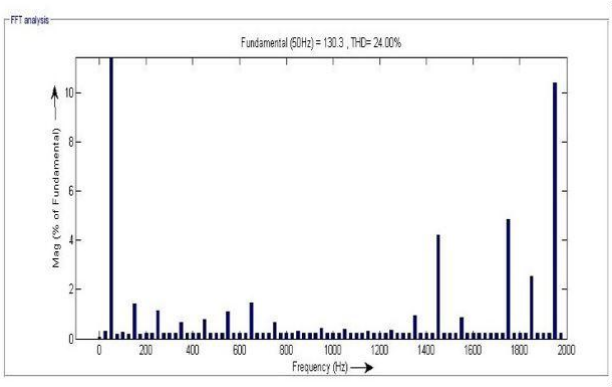


Figure 12. Harmonic profile of the inverter output voltage for M_a= 0.2Figure 13. Harmonic profile of the inverter output voltage for M_a= 0.4



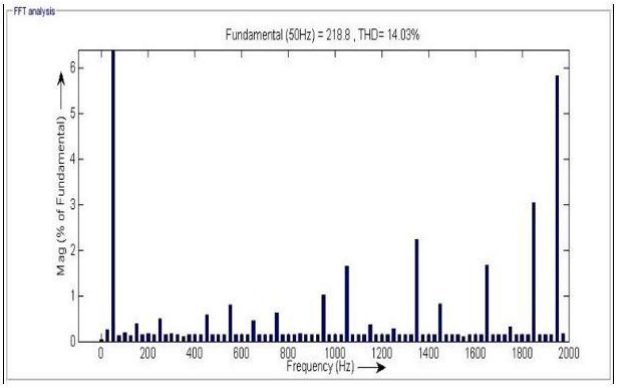


Figure 14. Harmonic profile of the inverter output voltage for M_a= 0.6Figure 15. Harmonic profile of the inverter output voltage for M_a= 0.8

The proposed inverter configuration inherently exhibited the characteristics of the full-bridge 3-, 5- and 7-level inverter topologies within the range of the modulation index: 0.2 ≤Ma < 0.75. Beyond the modulation index value of 0.75, 9-level voltage waveform is synthesized at the output of the topology.

3.2. ExperimetalResults –

Based on the simulation results, a laboratory prototype of thenine-level multilevel PWM inverter was set-up and tested to verify its validity. Figure 17shows the laboratory prototype set-up of the proposed inverter and Table IIgives the prototype specifications and parameters.The PWM signals generated in Matlab/Simulink is fed to the 9 level inverter by interfacing the Matlab/Simulink using Arduino Uno. The gate pulses generated using the Arduino Uno Microcontroller is having only a 5V magnitude. So in order toconvert it into the required voltage level a gate driver circuit is required. Gate driver circuit used here uses a IRS2110. The hardware setup for the entire system is developed. The experimental results are tested by using a digital storage oscilloscope.

Table II.Components rating:

Components	Specification
Driver IRS2110	500V, 2.5A
IGBT 1B16AJ	1200V, 25A
Arduino UNO Rev3	5V, 40mA
Capacitor	2200µF
Voltage Regulator LM7805	Input voltage: (7V-35V), Regulated output: 5V (4.8V-5.2V)
Resistor	50Ω

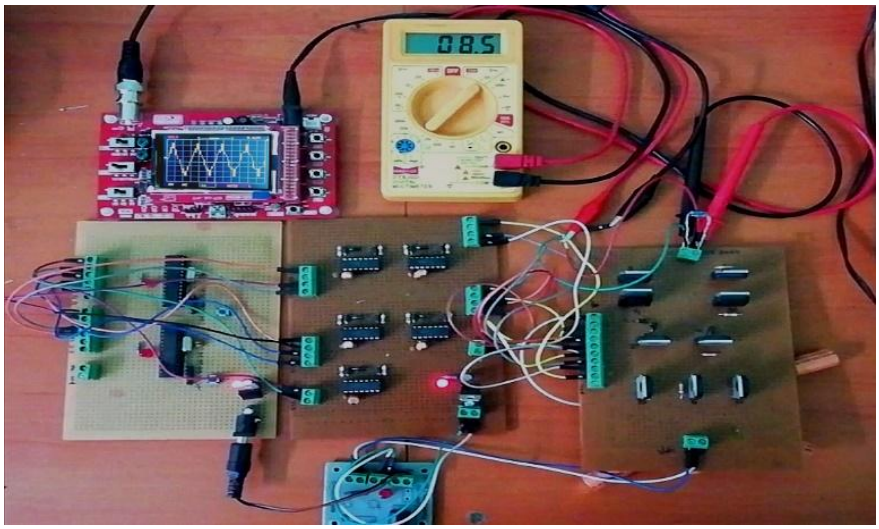


Figure 16. Complete Hardware Setup of the Inverter

4. CONCLUSION

A multilevel PWM inverter which can effectively increase the number of output voltage levels with a single dc voltage source is presented here. The operational principles, modulation scheme and switching functions have been analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage has been achieved. The proposed multilevel inverter exhibited the behaviour of 3-, 5-, 7- and 9-level inverters. In order to synthesize output voltage level, the proposed multilevel inverter needs a single dc voltage source with a series connection of four capacitors, three diodes, nine active switches for synthesizing output voltage levels, and an H-bridge cell. For a typical modulation index of 0.8, a THD value of 14.03% has been achieved in the output voltage waveform of the proposed inverter configuration. The performance of the proposed inverter topology has been presented through simulations and experiments for an R–L load; results have been adequately presented.

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